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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,461	12/16/2003	Li-Shin Huang	AITP0005USA	1460

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EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,461	HUANG, LI-SHIN	
	Examiner	Art Unit	
	Kevin M. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-8, 11-13 and 16-18** are rejected under 35 U.S.C. 102(b) as being anticipated by **Kudo et al** (US 6,353,435) hereinafter **Kudo '435**.

3. As to **claim 1**, **Kudo '435** teaches a display controller for producing a multi-gradation image on a display device formed by a plurality of binary-state pixels in an array through a plurality of consecutive frames, the plurality of binary-state pixels being classified into a plurality of pixel groups having an identical size, the display controller comprising:

column addressing means for designating a column number of a desired pixel *[a column driver addresses a column number of displayed pixels, see col. 7, line 64--col. 8, line 7];*

row addressing means for designating a row number of the desired pixel *[a row driver addresses a row number of displayed pixels, see col. 7, line 64--col. 8, line 7];*

an image memory for providing gradation data in response to the column and row numbers of the desired pixel, the gradation data being indicative of a gradation level to be produced at the desired pixel *[a frame memory 8 provides gray-scale data to the column and row for displaying, fig. 1];*

a waveform pattern memory for providing the display device with plural sets of waveform pattern signals, each set having an identical number of waveform pattern signals, each waveform pattern signal having a predetermined number of bits and producing a different gradation level when applied to a pixel, each bit being provided for displaying during a corresponding frame of the plurality of consecutive frames *[a gray-scale No. 1 through No. 64 pattern generator are within the FRC pattern generator 107 in figure 4, col. 9, lines 31-63]*; and

a waveform pattern selector for outputting a waveform pattern selecting signal in response to the column and row numbers of the desired pixel such that the waveform pattern memory provides two adjacent pixel groups with two different sets of the plural sets of waveform pattern signals, respectively *[a write data selector 106 for selecting FRC decoders 101-104, fig. 3, col. 9, lines 20-30]*, wherein:

the waveform pattern memory determines a selected set of the plural sets of waveform pattern signals in response to the waveform pattern selecting signal, determines a selected waveform pattern signal of the selected set of waveform pattern signals in response to the gradation data, and provides the bits of the selected waveform pattern signal, one bit per frame, over the plurality of consecutive frames *[said gray-scale No. 1 through No. 64 pattern generator determine a selected set of patterns such as a gray-scale No. 1 pattern 107 is consecutive a gray-scale No.2 pattern 107 in accordance with said write data selector 106, fig. 4, col. 9, lines 31-41]*;

the two different sets of the plural sets of waveform pattern signals provided for the two adjacent pixel groups, respectively, are so designed as to operate the two

adjacent pixel groups at two different states during at least one frame of the plurality of consecutive frames; and the plurality of consecutive frames is displayed at a frame rate high enough for preventing visual disturbances *[said gray-scale No. 1 pattern 107 and said gray-scale No.2 pattern 107 are two different sets, which are operated at the high frame rate by the frame rate control (FRC) 21, and are displayed on the screen of the LCD, see figs.2-6, col. 3, lines 40-46 and col. 9, line 6 through col. 10, line 67].*

4. As to claim 2, the display controller according to claim 1, wherein: the frame rate is equal to or higher than 120 Hz, whereas **Kudo '435** conventionally discloses in col. 1, lines 22-26.

5. As to claim 3, the display controller according to claim 1, wherein: the frame rate is equal to or higher than (2^n x 15) Hz where n is equal to or larger than 3, whereas Kudo conventionally discloses in col. 1, lines 27-30.

6. As to claim 4, the display controller according to claim 1, wherein: the waveform pattern memory is restricted to provide only two sets of waveform pattern signals, whereas **Kudo '435** conventionally discloses the frame rate is set equal to or higher than (2^n x 15) Hz. Under such a condition, any two frames with the same frame serial number among the two consecutive 2^n-gradation images (2^n gray-scale images) are displayed at a rate equal to or higher than 15 Hz, i.e., once every 2^n frames in col. 1, lines 27-30.

7. As to claim 5, the display controller according to claim 4, wherein: the waveform pattern memory stores a first set of the two sets of waveform pattern signals and derives a second set of the two sets of waveform pattern signals from the first set of the

two sets of waveform pattern signals by using the waveform pattern selecting signal, whereas **Kudo '435** conventionally discloses the frame rate is set equal to or higher than (2^n x 15) Hz. Under such a condition, any two frames with the same frame serial number among the two consecutive 2^n-gradation images (2^n gray-scale images) are displayed at a rate equal to or higher than 15 Hz, i.e., once every 2^n frames in col. 1, lines 27-30.

8. As to claim 6, the display controller according to claim 4, wherein: the waveform pattern selecting signal is a binary selecting signal, which is restricted to select between the two sets of waveform pattern signals, whereas **Kudo '435** conventionally discloses the frame rate is set equal to or higher than (2^n x 15) Hz. Under such a condition, any two frames with the same frame serial number among the two consecutive 2^n-gradation images (2^n gray-scale images) are displayed at a rate equal to or higher than 15 Hz, i.e., once every 2^n frames in col. 1, lines 27-30.

9. As to claim 7, the display controller according to claim 4, wherein: the multi-gradation image has 2^m gradations [2^m gray levels, 64 gray-scale=2^6 gray-scale] and is produced through consecutive 2^n frames where m is equal to or smaller than n and n is equal to or larger than 3, and each set of the two sets of waveform pattern signals has 2^m waveform pattern signals for producing the 2^m gradations, respectively, each waveform pattern signal having 2^n bits, whereas **Kudo '435** teaches in col. 9, line 64—col. 10, line 50.

10. As to claim 8, the display controller according to claim 7, wherein: the frame rate is equal to or higher than (2^n x15) Hz, whereas **Kudo '435** conventionally discloses in col. 1, lines 27-30.

11. As to claim 11, the display controller according to claim 1, wherein: each of the plurality of pixel groups is formed by a single pixel of the plurality of binary-state pixels, whereas **Kudo '435** teaches in col. 9, lines 33-38.

12. As to claim 12, the display controller according to claim 1, wherein: the display device is a color display device such that each of the plurality of binary-state pixels is constructed to produce one of three primary colors: red, green, and blue, and each of the plurality of pixel groups is formed by a single pixel of the plurality of binary-state pixels regardless of its color, whereas **Kudo '435** teaches in col. 9, lines 6-19.

13. As to claim 13, the display controller according to claim 1, wherein: the display device is a color display device such that every three pixels of the plurality of binary-state pixels makes up a color pixel unit and produces three primary colors: red, green, and blue, respectively, and each of the plurality of pixel groups is formed by a single one of the color pixel units, whereas **Kudo '435** teaches in col. 9, lines 6-19.

14. As to claim 16, the display controller according to claim 1, wherein: the column addressing means is implemented by a pixel counter, whereas **Kudo '435** teaches in col. 7, line 64 –col. 8, line 7, a data driver which is a pixel counter.

15. As to claim 17, the display controller according to claim 1, wherein: the row addressing means is implemented by a scan line counter, whereas **Kudo '435** teaches in col. 7, line 64 –col. 8, line 7, a scan driver which is a scan line counter.

16. As to claim 18, the display controller according to claim 1, further comprising: a frame counter for sequentially indicating the waveform pattern memory with each of the plurality of consecutive frames, whereas **Kudo '435** teaches a frame rate control (FRC) which is a fame counter.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kudo '435** in view of **Saxena** et al (US 5,777,590).

19. As to claim 9, **Kudo '435** teaches all of the claimed limitation, except wherein the waveform pattern selector outputs the waveform pattern selecting signal in response to a least significant bit of the column number and a least significant bit of the row number.

However, **Saxena** teaches a LCD controller which includes least significant 4 bits of the row counter and least significant 4 bits of the column counter, see col. 9, lines 15-56.

As to claim 10, **Saxena** teaches a logic circuit for accomplishing this phase shift and including exclusive-OR gate 84, see fig. 4, col. 5, lines 6-12.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the LCD controller of **Kudo '435** to include the least

significant 4 bits of the row counter and least significant 4 bits of the column counter as taught by Saxena in order to achieve the benefit of providing stable grayscale patterns on standard LCD's without any visual shimmering effect (see col. 9, lines 65-col. 10, lines 57).

20. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kudo '435** in view of **Lin** (US 6,791576).

Kudo '435 teaches all of the claimed limitation of claim 1, except for a look-up table coupled between the image memory and the waveform pattern memory for transferring the gradation data provided by the image memory, thereby expanding the number of bits of the gradation data; and a look-up table coupled between the image memory and the waveform pattern memory for transferring the gradation data provided by the image memory, thereby performing Gamma corrections on the gradation data.

However, **Lin** teaches a table of segments in a gamma correction function using dual level mapping having input W with multi-bit value that is normalized between 0 and 1 in fig. 5, col. 5, lines 55 for further details.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the table of segments in the gamma correction as taught by **Lin** in the LCD controller of **Kudo '435** in order to achieve the benefit of improving high precision gamma correction of pixels, while fabricating a driver circuitry at low cost (see col. 11, lines 30-col. 12, lines 8 of Lin).

21. Claims 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kudo et al (US 6,084,561) hereinafter **Kudo '561**.

As to claim 19, figure 9 of **Kudo '561** teaches a method of producing a multi-gradation image on a display device formed by a plurality of binary-state pixels in an array through a plurality of consecutive frames, comprising: defining an elementary 2x2 pixel cell on the display device, the elementary 2x2 pixel cell having two pixels along a first diagonal and two pixels along a second diagonal; defining a first set of waveform pattern signals and a second set of waveform pattern signals, each set having an identical number of waveform pattern signals, each waveform pattern signal having a predetermined number of bits and producing a different gradation level when applied to a pixel, each bit being provided for displaying during a corresponding frame of the plurality of consecutive frames; providing the two pixels along the first diagonal with the first set of waveform pattern signals and the two pixels along the second diagonal with the second set of waveform pattern signals such that the two pixels along the first diagonal and the two pixels along the second diagonal are operated at different states during at least one frame of the plurality of consecutive frames; and displaying the plurality of consecutive frames at a frame rate high enough for preventing visual disturbances in col. 5, lines 12-19, and col. 7, lines 27-57.

22. As to claim 20, **Kudo '561** teaches the method according to claim 19, wherein: the multi-gradation image has 2^m gradations (2^m gray-scales)and is produced through consecutive 2^n frames where m is equal to or smaller than n and n is equal to or larger than 3; each set of the first and second sets of waveform pattern signals has 2^m waveform pattern signals for producing the 2^m gradations (2^m gray-scales), respectively,

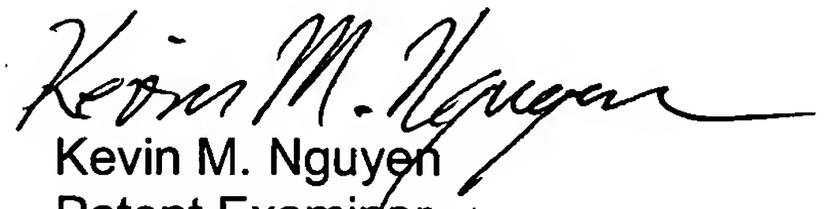
each waveform pattern signal having 2^n bits; and the frame rate is equal to or higher than (2n x 15) Hz in col. 4, lines 11-39.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. NGUYEN whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, a supervisor RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Art Unit 2629

KMN
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